Lecture 7: Table-Based \( (g_m/I_D) \) Design

Sebastian Hoyos
Analog & Mixed-Signal Center
Texas A&M University
Announcements

• Reading
  • Will post $g_m/I_D$ paper
    • Material is only supplementary reference

• HW2 due Monday 9:10AM

• Exam 1 Friday Sept. 30
Agenda

• Technology characterization for design
• Table-based \((g_m/I_D)\) design example
• Adapted from Prof. B. Murmann (Stanford) notes
How to Design with Modern Sub-Micron (Nanometer) Transistors?

• Hand calculations with square-law model can deviate significantly from actual device performance
  • However, advanced model equations are too tedious for design

• Tempts designers to dive straight to simulation with little understanding on circuit performance trade-offs
  • “Spice Monkey” approach

• How can we accurately design when hand analysis models are way off?

• Employ a design methodology which leverages characterization data from BSIM simulations
The Problem

Specifications

Square Law → Hand Calculations

BSIM → Circuit

Spice → Results

[Murmann]
The Solution

BSIM → Spice → Design Charts → Hand Calculations → Specifications

BSIM → Spice → Results

Circuit

[Murmann]
Technology Characterization for Design

• Generate data for the following over a reasonable range of $g_m/I_D$ and channel lengths
  • Transit frequency ($f_T$)
  • Intrinsic gain ($g_m/g_{ds}$)
  • Current density ($I_D/W$)

• Also useful is extrinsic capacitor ratios
  • $C_{gd}/C_{gg}$ and $C_{dd}/C_{gg}$

• Parameters are (to first order) independent of transistor width, which enables “normalized design”

• Do design hand calculations using the generated technology data

• Still need to understand how the circuit operates for an efficient design!!!
$G_m/I_D$ vs $V_{ov}$, $W=6\,\mu m$, $V_{DS}=1.5\,V$
Gain

NMOS Gain ($g_m/g_o$) vs $V_{ov}$, $W=6\,\mu m$, $V_{DS}=1.5\,V$

NMOS Gain ($g_m/g_o$) vs $g_m/l_D$, $W=6\,\mu m$, $V_{DS}=1.5\,V$
\( f_T \)

**NMOS** \( f_T \) \( (g_m/C_{g} \) vs \( V_{ov} \), \( W=6\mu m, V_{DS}=1.5V \)

- **L=0.6\mu m**
- **L=1.2\mu m**
- **L=2.4\mu m**

**NMOS** \( f_T \) \( (g_m/C_{g} \) vs \( g_m/l_D \), \( W=6\mu m, V_{DS}=1.5V \)

- **L=0.6\mu m**
- **L=1.2\mu m**
- **L=2.4\mu m**
ID/W

NMOS $I_D/W$ vs $V_{GS}$. $W=6\mu m$, $V_{DS}=1.5V$

<table>
<thead>
<tr>
<th>$L$ (um)</th>
<th>$I_D/W$ (A/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>2.4</td>
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</tbody>
</table>

NMOS Current Density ($I_D/W$) vs $g_m/I_D$. $W=6\mu m$, $V_{DS}=1.5V$

<table>
<thead>
<tr>
<th>$g_m/I_D$ (V$^{-1}$)</th>
<th>$L=0.6\mu m$</th>
<th>$L=1.2\mu m$</th>
<th>$L=2.4\mu m$</th>
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</table>
CS Amplifier Design Example

- Specifications
  - 0.6µm technology
  - |A_v| ≥ 4V/V
  - f_u ≥ 100MHz
  - C_L = 5pF
  - Vdd = 3V
CS Amplifier Small-Signal Model (No $R_S$)

\[ \frac{v_o}{v_i} = \frac{(sC_{gd} - g_m)R_p}{s(C_L + C_{gd} + C_{db})R_p + 1}, \text{ where } R_p = \frac{r_o R_L}{r_o + R_L} \]

\[ \omega_z = \frac{g_m}{C_{gd}} \quad (\text{located at very high frequency, } > \omega_T) \]

\[ \omega_p = -\frac{1}{R_p(C_L + C_{gd} + C_{db})} \approx -\frac{1}{R_L C_L} \]

\[ A_v = -g_m R_p \approx -g_m R_L \]

\[ \omega_u = A_v \omega_p \approx \frac{g_m}{C_L} \]
Design Procedure

1. Determine $g_m$ from design specifications
   a. $\omega_u$ in this example

2. Pick transistor L
   a. Short channel $\rightarrow$ high $f_T$ (high bandwidth)
   b. Long channel $\rightarrow$ high $r_o$ (high gain)

3. Pick $g_m/I_D$ (or $f_T$)
   a. Large $g_m/I_D$ $\rightarrow$ low power, large signal swing (low $V_{ov}$)
   b. Small $g_m/I_D$ $\rightarrow$ high $f_T$ (high speed)
   c. May also be set by common-mode considerations

4. Determine $I_D/W$ from $I_D/W$ vs $g_m/I_D$ chart

5. Determine $W$ from $I_D/W$

• Other approaches exist
1. Determine $g_m$ (& $R_L$)

- From $\omega_u$ and DC gain specification

\[ \omega_u = A_v \omega_p \approx \frac{g_m}{C_L} \]
\[ g_m = \omega_u C_L = 2\pi(100\,MHz)(5\,pF) = 3.14mA/V \]

Note, this may be slightly low due to neglecting $C_{gd}$ and $C_{db}$

\[ A_v = -g_m R_\parallel \approx -g_m R_L \]
\[ R_L = \frac{A_v}{g_m} \]

Adding 20% margin to compensate for $r_o$ effects
\[ R_L = \frac{A_v}{g_m} = \frac{4.8}{3.14mA/V} = 1.5k\Omega \]
2. Pick Transistor L

- Need to look at gain and $f_T$ plots

NMOS Gain ($g_m/g_o$) vs $g_m/I_D$, $W=6\mu m$, $V_{DS}=1.5V$

NMOS $f_T$ ($g_m/C_{gg}$) vs $g_m/I_D$, $W=6\mu m$, $V_{DS}=1.5V$

- Since amplifier $A_V \geq 4$, min channel length ($L=0.6\mu m$) will work with $g_m/I_D \sim > 2$
  - Min channel length provides highest $f_T$ at this $g_m/I_D$ setting
3. Pick $g_m/I_D$ (or $f_T$)

- Setting $I_D$ for $V_O=1.5V$ for large output swing range

\[ I_D = \frac{3V - 1.5V}{1.5k\Omega} = 1mA \]

\[ V_o = 1.5V \]

\[ g_m = \frac{3.14mA/V}{1mA} = 3.14V^{-1} \]
Verify Transistor Gain & $f_T$ at $g_m/I_D$ Setting

- Transistor gain = 30.6 >> amplifier $A_v \geq 4$
- Transistor $f_T = 6.7$GHz >> amplifier $f_u = 100$MHz
- $g_m/I_D$ setting is acceptable
4. Determine Current Density ($I_D/W$)

- $g_m/I_D = 3.14 V^{-1}$ maps to a current density of $20.2 \mu A/\mu m$

- Verify current density is achievable at a reasonable $V_{GS}$

- $V_{GS} = 1.15 V$ is reasonable with $V_{dd} = 3 V$ & $V_{DS} = 1.5 V$
5. Determine Transistor W from $I_D/W$

• From Step 3, we determined that $I_D=1\text{mA}$

$$W = \frac{I_D}{(I_D/W)} = \frac{1\text{mA}}{20.2\mu\text{A}/\mu\text{m}} = 49.5\mu\text{m}$$

• For layout considerations and to comply with the technology design rules
  • Adjust 49.5μm to 49.2μm and realize with 8 fingers of 6.15μm
  • This should match our predictions well, as the charts are extracted with a 6μm device
    • Although it shouldn’t be too sensitive to exact finger width
Simulation Circuit

![Simulation Circuit Diagram](image)

- **vdd**: 3
- **i**: -999u
- **vdc**: 1.153
- **v0**: 1.153
- **vgs**: 1.153
- **vds**: 1.502
- **R0**: 3
- **v**: 1.498
- **i**: 999u
- **pwr**: 1.497m
- **out**: 1.502
- **N0**: 1.502
- **id**: 998.9u
- **vds**: 1.502
- **gnd**: 0

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Operating Point Information

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<th>3.14mA/V</th>
<th>3.14V⁻¹</th>
<th>1mA</th>
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Total Cgate = Cgg = 74.1fF

Total Cdrain = Cdd + Cjd = 12.5fF + 55.6fF = 68.1fF

Total Csource = Css + Cjs = 43.2fF + 0fF = 43.2fF
AC Response

- Design is very close to specs
- Discrepancies come from neglecting $r_o$ and $C_{drain}$
- With design table information we can include estimates of these in our original procedure for more accurate results
Next Time

• Current Mirrors